DATA SHEET

74HCT9046A
PLL with band gap controlled VCO

Product specification
Supersedes data of 1999 Jan 11

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Philips
Semiconductors

PHILIPS

PLL with band gap controlled VCO 74HCT9046A

FEATURES

- Operation power supply voltage range from 4.5 to 5.5 V
- Low power consumption
- Inhibit control for ON/OFF keying and for low standby power consumption
- Centre frequency up to 17 MHz (typical) at V_{CC} = 5.5 V
- Choice of two phase comparators:
  - PC1: EXCLUSIVE-OR
  - PC2: Edge-triggered JK flip-flop.
- No dead zone of PC2
- Charge pump output on PC2, whose current is set by an external resistor R_b
- Centre frequency tolerance ±10%
- Excellent Voltage Controlled Oscillator (VCO) linearity
- Low frequency drift with supply voltage and temperature variations
- On-chip band gap reference
- Glitch free operation of VCO, even at very low frequencies
- Zero voltage offset due to op-amp buffering
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.

APPLICATIONS

- FM modulation and demodulation where a small centre frequency tolerance is essential
- Frequency synthesis and multiplication where a low jitter is required (e.g. video picture-in-picture)
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

GENERAL DESCRIPTION

The 74HCT9046A is a high-speed Si-gate CMOS device. It is specified in compliance with “JEDEC standard no 7A”.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
f_c	VCO centre frequency	C1 = 40 pF; R1 = 3 kΩ; V_{CC} = 5 V	16	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   N = total load switching outputs;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. Applies to the phase comparator section only (pin INH = HIGH). For power dissipation of the VCO and demodulator sections see Figs 26 to 28.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74HCT9046AN	16	DIL16	plastic	SOT38Z
74HCT9046AD	16	SO16	plastic	SOT109A

PINNING

PIN	SYMBOL	DESCRIPTION
1	GND	ground (0 V) of phase comparators
2	PC1_OUT/ PCP_OUT	phase comparator 1 output or phase comparator pulse output
3	COMP_IN	comparator input
4	VCO_OUT	VCO output
5	INH	inhibit input
6	C1A	capacitor C1 connection A
7	C1B	capacitor C1 connection B
8	GND	ground (0 V) VCO
9	VCO_IN	VCO input
10	DEM_OUT	demodulator output
11	R1	resistor R1 connection
12	R2	resistor R2 connection
13	PC2_OUT	phase comparator 2 output; current source adjustable with R_b
14	SIG_IN	signal input
15	RB	bias resistor (R_b) connection
16	V_{CC}	supply voltage

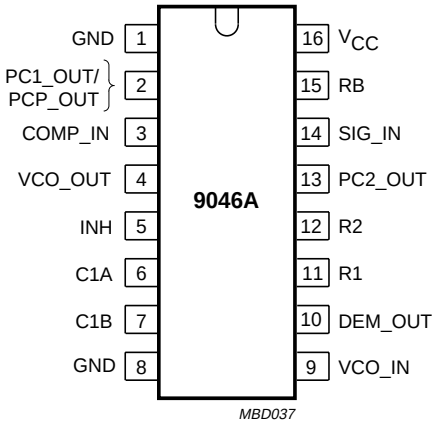


Fig.1 Pin configuration.

LOGIC AND FUNCTIONAL SYMBOLS AND DIAGRAMS

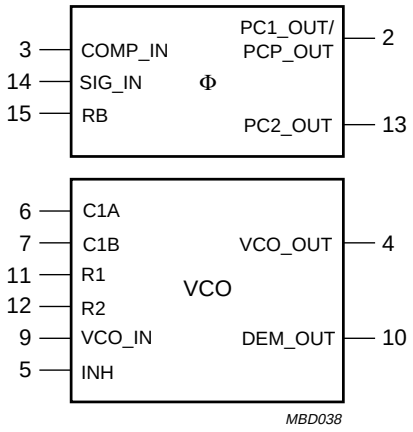


Fig.2 Logic symbol.

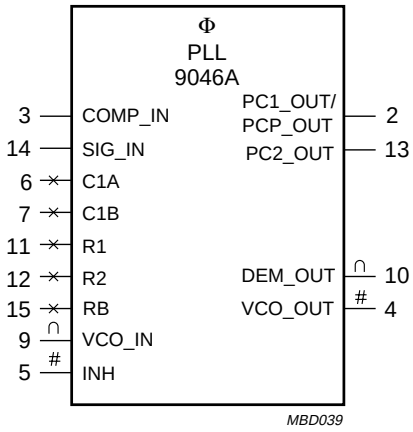


Fig.3 IEC logic symbol.

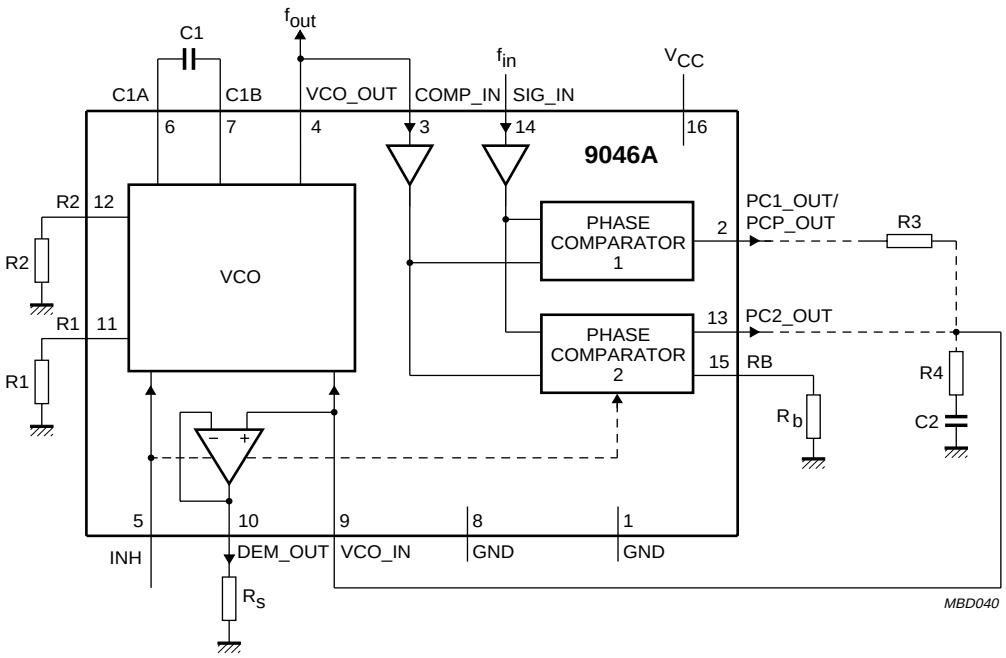


Fig.4 Block diagram.

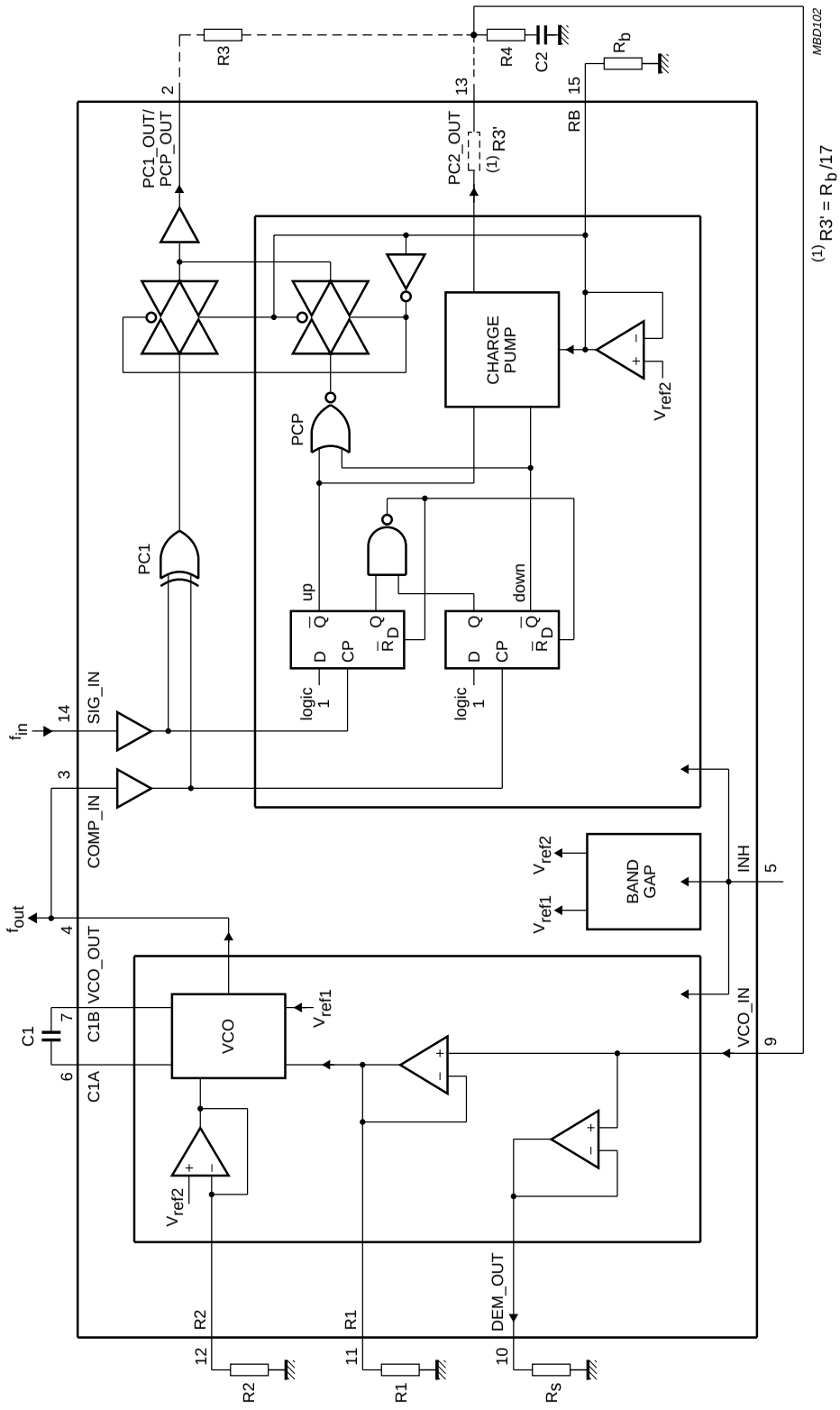


Fig.5 Logic diagram.

FUNCTIONAL DESCRIPTION

The 74HCT9046A is a phase-locked-loop circuit that comprises a linear VCO and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input (see Fig.4). The signal input can be directly coupled to large voltage signals (CMOS level), or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 74HCT9046A forms a second-order loop PLL.

The principle of this phase-locked-loop is based on the familiar 74HCT4046A. However extra features are built-in, allowing very high-performance phase-locked-loop applications. This is done, at the expense of PC3, which is skipped in this 74HCT9046A. The PC2 is equipped with a current source output stage here. Further a band gap is applied for all internal references, allowing a small centre frequency tolerance. The details are summed up in the next section: “Differences with respect to the familiar 74HCT4046A”. If one is familiar with the 74HCT4046A already, it will do to read this section only.

Differences with respect to the familiar 74HCT4046A

- A centre frequency tolerance of maximum ±10%.
- The on board band gap sets the internal references resulting in a minimal frequency shift at supply voltage variations and temperature variations.
- The value of the frequency offset is determined by an internal reference voltage of 2.5 V instead of $V_{CC} - 0.7$ V. In this way the offset frequency will not shift over the supply voltage range.
- A current switch charge pump output on pin PC2_OUT allows a virtually ideal performance of PC2. The gain of PC2 is independent of the voltage across the low-pass filter. Further a passive low-pass filter in the loop achieves an active performance. The influence of the parasitic capacitance of the PC2 output plays no role here, resulting in a true correspondence of the output correction pulse and the phase difference even up to phase differences as small as a few nanoseconds.
- Because of its linear performance without dead zone, higher impedance values for the filter, hence lower C-values, can now be chosen. Correct operation will not be influenced by parasitic capacitances as in the instance with voltage source output of the 4046A.
- No PC3 on pin RB but instead a resistor connected to GND, which sets the load/unload currents of the charge pump (PC2).
- Extra GND pin 1 to allow an excellent FM demodulator performance even at 10 MHz and higher.
- Combined function of pin PC1_OUT/PCP_OUT. If pin RB is connected to V_{CC} (no bias resistor R_b) pin PC1_OUT/PCP_OUT has its familiar function viz. output of PC1. If at pin RB a resistor (R_b) is connected to GND it is assumed that PC2 has been chosen as phase comparator. Connection of R_b is sensed by internal circuitry and this changes the function of pin PC1_OUT/PCP_OUT into a lock detect output (PCP_OUT) with the same characteristics as PCP_OUT of pin 1 of the 74HCT4046A.
- The inhibit function differs. For the HCT4046A a HIGH level at the inhibit input (pin INH) disables the VCO and demodulator, while a LOW level turns both on. For the 74HCT9046A a HIGH level on the inhibit input disables the whole circuit to minimize standby power consumption.

VCO

The VCO requires one external capacitor C1 (between pins C1A and C1B) and one external resistor R1 (between pins R1 and GND) or two external resistors R1 and R2 (between pins R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required (see Fig.5).

The high input impedance of the VCO simplifies the design of the low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin DEM_OUT. The DEM_OUT voltage equals that of the VCO input. If DEM_OUT is used, a load resistor (R_s) should be connected from pin DEM_OUT to GND; if unused, DEM_OUT should be left open. The VCO output (pin VCO_OUT) can be connected directly to the comparator input (pin COMP_IN), or connected via a frequency divider. The output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (pin INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

Phase comparators

The signal input (pin SIG_IN) can be directly coupled to the self-biasing amplifier at pin SIG_IN, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

PHASE COMPARATOR 1 (PC1)

This circuit is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is: $V_{DEM\_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$

where:

V_{DEM_OUT} is the demodulator output at pin DEM_OUT.

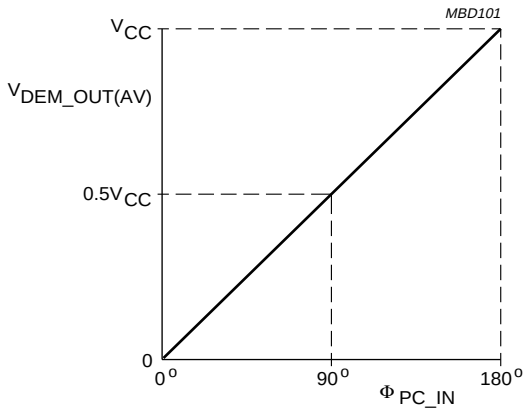
$V_{DEM\_OUT} = V_{PC1\_OUT}$ (via low-pass).

The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi}(V/r)$.

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin DEM_OUT (V_{DEM_OUT}), is the resultant of the phase differences of signals (SIG_IN) and the comparator input (COMP_IN) as shown in Fig.6. The average of V_{DEM_OUT} is equal to $0.5V_{CC}$ when there is no signal or noise at SIG_IN and with this input the VCO oscillates at the centre frequency (f_c). Typical waveforms for the PC1 loop locked at f_c are shown in Fig.7. This figure also shows the actual waveforms across the VCO capacitor at pins C1A and C1B (V_{C1A} and V_{C1B}) to show the relation between these ramps and the VCO_OUT voltage.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of the input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behaviour of this type of phase comparator is that it may lock to input frequencies close to the harmonics of the VCO centre frequency.



$V_{DEM\_OUT} = V_{PC1\_OUT} = \frac{V_{CC}}{\pi}(\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$

$\Phi_{PC\_IN} = (\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$

Fig.6 Phase comparator 1; average output voltage as a function of input phase difference.

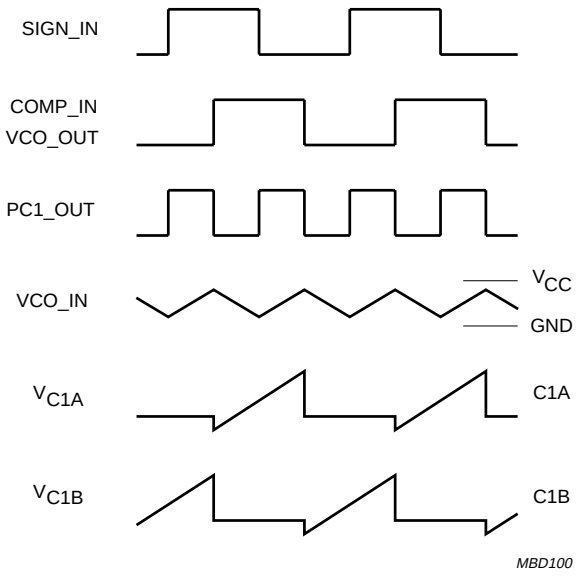


Fig.7 Typical waveforms for PLL using phase comparator 1; loop-locked at f_c.

PHASE COMPARATOR 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_IN and COMP_IN are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage with sink and source transistors acting as current sources, henceforth called charge pump output of PC2. The circuit functions as an up-down counter (see Fig.5) where SIG_IN causes an up-count and COMP_IN a down count. The current switch charge pump output allows a virtually ideal performance of PC2, due to appliance of some pulse overlap of the up and down signals. See Fig.8a.

The pump current I_P is independent from the supply voltage and is set by the internal band gap reference of 2.5 V.

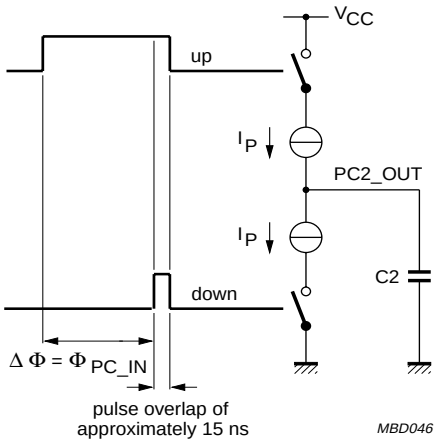
$$I_P = 17 \times \frac{2.5}{R_b}(A)$$

Where R_b is the external bias resistor between pin RB and ground.

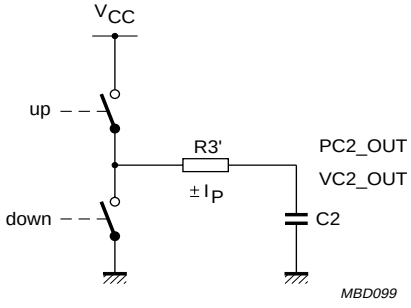
The current and voltage transfer function of PC2 are shown in Fig.9.

The phase comparator gain is:

$$K_p = \frac{|I_P|}{2\pi}(A/r)$$

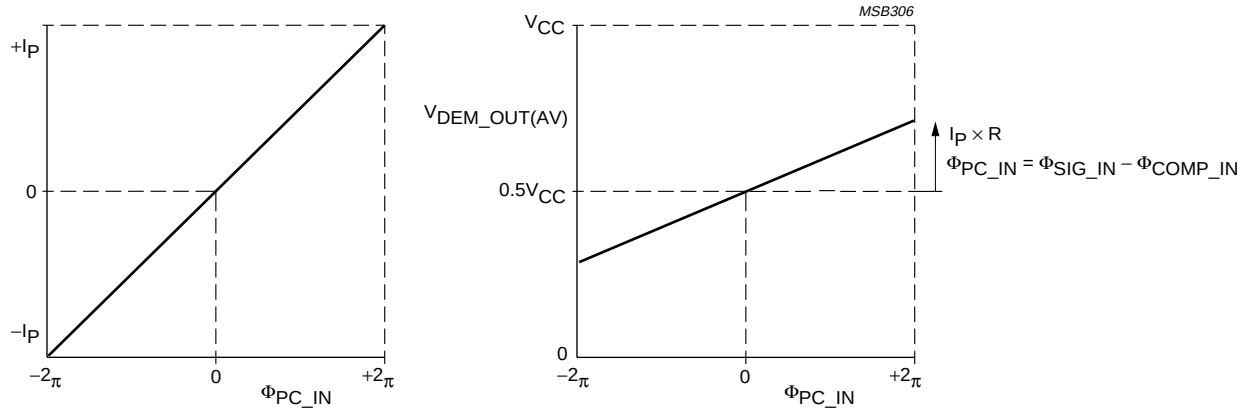


a. At every ΔΦ, even at zero ΔΦ both switches are closed simultaneously for a short period (typically 15 ns).



b. Comparable voltage-controlled switch.

Fig.8 The current switch charge pump output of PC2.



Two kinds of transfer functions may be regarded:

a. The current transfer:

pump current $\frac{|I_P|}{2\pi}\Phi_{PC\_IN}$

b.The voltage transfer; this transfer can be observed at PC2_OUT by connecting a resistor (R = 10 kΩ) between PC2_OUT and $0.5V_{CC}$;

$V_{DEM\_OUT} = V_{PC2\_OUT} = \frac{5}{4\pi}\Phi_{PC\_IN}$.

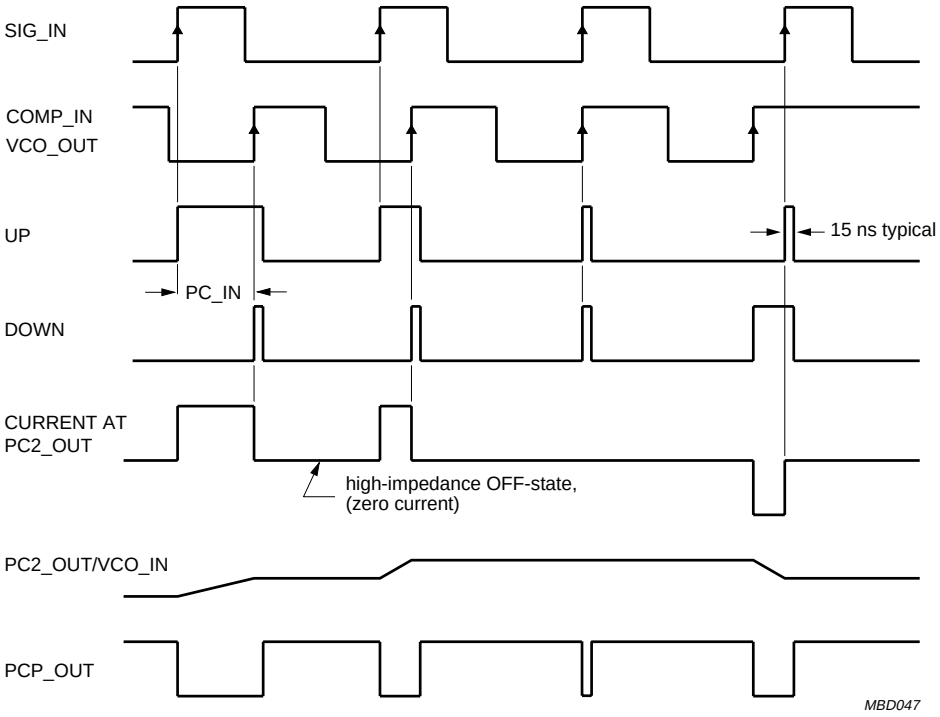
Fig.9 Phase comparator 2.

When the frequencies of SIG_IN and COMP_IN are equal but the phase of SIG_IN leads that of COMP_IN, the up output driver at PC2_OUT is held ‘ON’ for a time corresponding to the phase difference (Φ_{PC_IN}). When the phase of SIG_IN lags that of COMP_IN, the down or sink driver is held ‘ON’.

When the frequency of SIG_IN is higher than that of COMP_IN, the source output driver is held ‘ON’ for most of the input signal cycle time and for the remainder of the cycle time both drivers are ‘OFF’ (3-state). If the SIG_IN frequency is lower than the COMP_IN frequency, then it is the sink driver that is held ‘ON’ for most of the cycle. Subsequently the voltage at the capacitor (C2) of the low-pass filter connected to PC2_OUT varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition the signal at the phase comparator pulse output (PCP_OUT) has a minimum output pulse width equal to the overlap time, so can be used for indicating a locked condition.

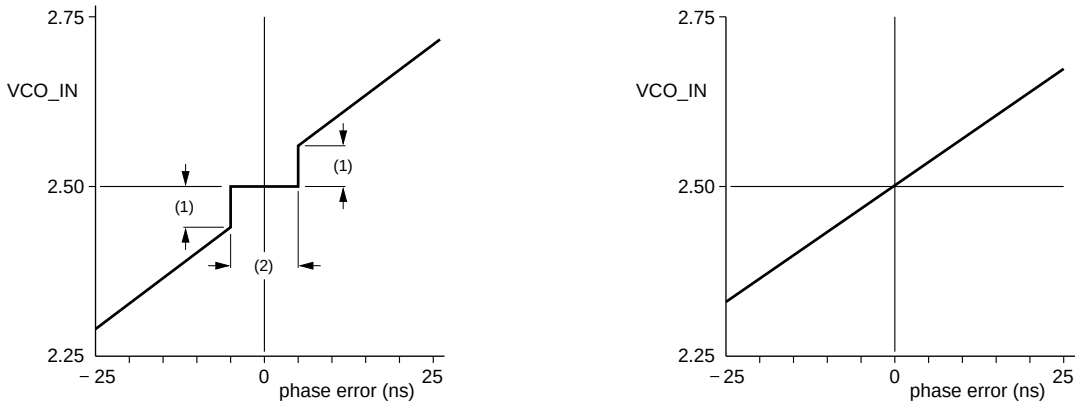
Thus for PC2 no phase difference exists between SIG_IN and COMP_IN over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_IN the VCO adjust, via PC2, to its lowest frequency.

By using current sources as charge pump output on PC2, the dead zone or backlash time could be reduced to zero. Also, the pulse widening due to the parasitic output capacitance plays no role here. This enables a linear transfer function, even in the vicinity of the zero crossing. The differences between a voltage switch charge pump and a current switch charge pump are shown in Fig.11.



The pulse overlap of the up and down signals (typically 15 ns).

Fig.10 Timing diagram for PC2.



a. Response with traditional voltage-switch charge-pump PC2_OUT (74HCT4046A).

(1) Due to parasitic capacitance on PC2_OUT.

(2) Backlash time (dead zone).

b. Response with current switch charge-pump PC2_OUT as applied in the 74HCT9046A.

Fig.11 The response of a locked-loop in the vicinity of the zero crossing of the phase error.

The design of the low-pass filter is somewhat different when using current sources. The external resistor R3 is no longer present when using PC2 as phase comparator. The current source is set by R_b. A simple capacitor behaves as an ideal integrator now, because the capacitor is charged by a constant current. The transfer function of the voltage switch charge pump may be used. In fact it is even more valid, because the transfer function is no longer restricted for small changes only. Further the current is independent from both the supply voltage and the voltage across the filter. For one that is familiar with the low-pass filter design of the 74HCT4046A a relation may show how R_b relates with a fictive series resistance, called R3'.

This relation can be derived by assuming first that a voltage controlled switch PC2 of the 74HCT4046A is connected to the filter capacitance C2 via this fictive R3' (see Fig.8b). Then during the PC2 output pulse the charge current equals:

$$|I_P| = \frac{V_{CC} - V_{C2(0)}}{R3'}$$

With the initial voltage $V_{C2(0)}$ at:

$$0.5V_{CC} = 2.5\ V,\ |I_P| = \frac{2.5}{R3'}$$

As shown before the charge current of the current switch of the 74HCT9046A is:

$$|I_P| = 17 \times \frac{2.5}{R_b}$$

Hence:

$$R3' = \frac{R_b}{17}(\Omega)$$

Using this equivalent resistance R3' for the filter design the voltage can now be expressed as a transfer function of PC2; assuming ripple ($f_r = f_i$) is suppressed, as:

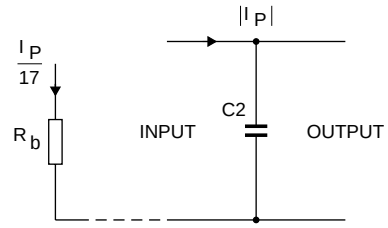
$$K_{PC2} = \frac{5}{4\pi}(V/r)$$

Again this illustrates the supply voltage independent behaviour of PC2.

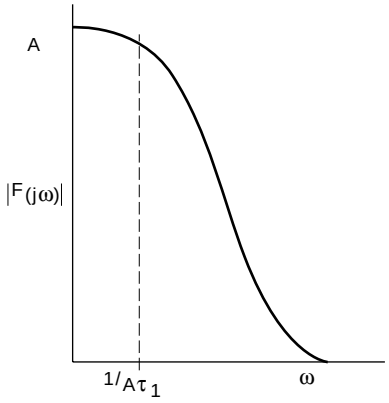
LOOP FILTER COMPONENT SELECTION

Examples of PC2 combined with a passive filter are shown in Figs 12 and 13. Figure 12 shows that PC2 with only a C2 filter behaves as a high-gain filter. For stability the damped version of Fig.13 with series resistance R4 is preferred.

Practical design values for R_b are between 25 and 250 kΩ with R3' = 1.5 to 15 kΩ for the filter design. Higher values for R3' require lower values for the filter capacitance which is very advantageous at low values the loop natural frequency ω_n.

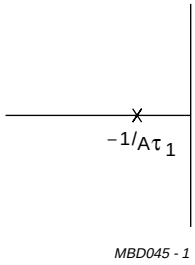


a. $\tau_1 = \frac{R_b}{17} \times C2 = R3' \times C2$



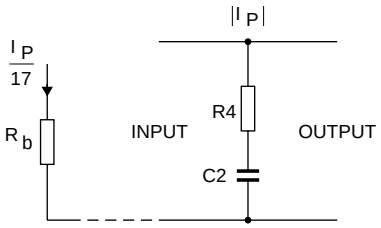
b. Amplitude characteristic:

$$F_{(j\omega)} = \frac{1}{1/A + j\omega\tau_1} \approx \frac{1}{j\omega\tau_1}$$



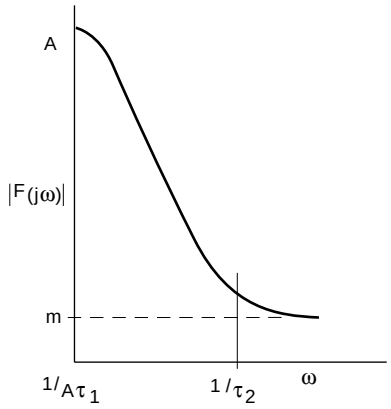
c. Pole zero diagram.

Fig.12 Simple loop filter for PC2 without damping.



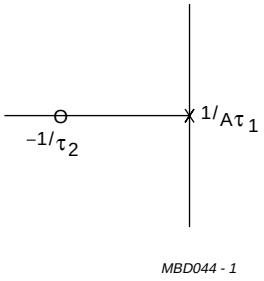
a. $\tau_1 = \frac{R_b}{17} \times C2 = R3' \times C2$

$\tau_2 = R4 \times C2$



b. Amplitude characteristic:

$$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1}$$



c. Pole zero diagram.
A = DC gain limit, due to leakage.

Fig.13 Simple loop filter for PC2 with damping.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC Characteristics	–40	–	+85	°C
			–40	–	+125	°C
t_r, t_f	input rise and fall times on pin INH	V_{CC} = 4.5 V	–	6	500	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	–	±20	mA
I_O	output source or sink current	$–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 to +125 °C			
	DIL16	note 1	–	750	mW
	SO16	note 2	–	500	mW

Notes

1. For DIL16 packages: above 70 °C derate linearly with 12 mW/K.
2. For SO16 packages: above 70 °C derate linearly with 8 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
PHASE COMPARATOR SECTION							
V_{IH}	HIGH-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	3.15	2.4	–	V
V_{IL}	LOW-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	–	2.1	1.35	V
V_{OH}	HIGH-level output voltage on pins PCP_OUT and PCn_OUT	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	4.5	3.98	4.32	–	V
V_{OL}	LOW-level output voltage on pins PCP_OUT and PCn_OUT	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	–	0	0.1	V
		I_O = –4.0 mA	4.5	–	0.15	0.26	V
I_{LI}	input leakage current in pins SIG_IN and COMP_IN	V_{CC} or GND	5.5	–	–	±30	μA
I_{OZ}	3-state OFF-state current in pin PC2_OUT	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±0.5	μA
R_I	input resistance SIG_IN, COMP_IN	V_I at self-bias operating point; ΔV_I = 0.5 V; see Figs 14 to 16	4.5	–	250	–	kΩ
R_b	bias resistance		4.5	25	–	250	kΩ
I_P	charge pump current	R_b = 40 kΩ	4.5	±0.53	±1.06	±2.12	mA
VCO SECTION							
V_{IH}	HIGH-level input voltage on pin INH	DC coupled	4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage on pin INH	DC coupled	4.5 to 5.5	–	1.2	0.8	V
V_{OH}	HIGH-level output voltage on pin VCO_OUT	V_I = V_{IH} or V_{IL}					
		I_O = –20 μA	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	4.5	3.98	4.32	–	V
V_{OL}	LOW-level output voltage on pin VCO_OUT	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.26	V
V_{OL}	LOW-level output voltage on pins C1A and C1B	V_I = V_{IH} or V_{IL}; I_O = 4.0 mA	4.5	–	–	0.40	V
I_{LI}	input leakage current in pins INH and VCO_IN	V_{CC} or GND	5.5	–	–	±0.1	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
R1	resistor value		4.5	3	–	300	kΩ
R2	resistor value		4.5	3	–	300	kΩ
C1	capacitance		4.5	40	–	no limit	pF
V_{VCO_IN}	operating voltage on pin VCO_IN	over the range specified for R1	4.5	1.1	–	3.4	V
			5.0	1.1	–	3.9	V
			5.5	1.1	–	4.4	V
DEMODULATOR SECTION							
R_s	resistor value	at R_s > 300 kΩ the leakage current can influence V_{DEM_OUT}	4.5	50	–	300	kΩ
V_{OFF}	offset voltage VCO_IN to V_{DEM_OUT}	$V_I = V_{VCO\_IN} = 0.5V_{CC}$; values taken over R_s range, see Fig.17	4.5	–	±20	–	mV
R_{dyn}	dynamic output resistance at DEM_OUT	$V_{DEM\_OUT} = 0.5V_{CC}$	4.5	–	25	–	Ω
GENERAL							
I_{CC}	quiescent supply current (disabled)	pin INH at V_{CC}	5.5	–	–	8.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	other inputs at V_{CC} or GND; $V_I = V_{CC} - 2.1$ V; note 1	4.5	–	100	360	μA
T_{amb} = −40 to +85 °C							
PHASE COMPARATOR SECTION							
V_{IH}	HIGH-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	3.15	–	–	V
V_{IL}	LOW-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	–	–	1.35	V
V_{OH}	HIGH-level output voltage on pins PCP_OUT and PCn_OUT	$V_I = V_{IH}$ or V_{IL}					
		I_O = –20 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	4.5	3.84	–	–	V
V_{OL}	LOW-level output voltage on pins PCP_OUT and PCn_OUT	$V_I = V_{IH}$ or V_{IL}					
		I_O = –20 μA	4.5	–	–	0.1	V
		I_O = –4.0 mA	4.5	–	–	0.33	V
I_{LI}	input leakage current in pins SIG_IN and COMP_IN	V_{CC} or GND	5.5	–	–	±38	μA
I_{OZ}	3-state OFF-state current PC2_OUT	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	±5.0	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
VCO SECTION							
V_{IH}	HIGH-level input voltage on pin INH	DC coupled	4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage on pin INH	DC coupled	4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage on pin VCO_OUT	$V_I = V_{IH}$ or V_{IL}					
		$I_O = –20$ μA	4.5	4.4	–	–	V
		$I_O = –4.0$ mA	4.5	3.84	–	–	V
V_{OL}	LOW-level output voltage on pin VCO_OUT	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 20$ μA	4.5	–	–	0.1	V
		$I_O = 4.0$ mA	4.5	–	–	0.33	V
V_{OL}	LOW-level output voltage on pins C1A and C1B	$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	4.5	–	–	0.47	V
I_{LI}	input leakage current in pins INH and VCO_IN	V_{CC} or GND	5.5	–	–	±1.0	μA
QUIESCENT SUPPLY CURRENT							
I_{CC}	quiescent supply current (disabled)	pin INH at V_{CC}	5.5	–	–	80.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	other inputs at V_{CC} or GND; $V_I = V_{CC} – 2.1$ V; note 1	4.5	–	–	450	μA
T_{amb} = –40 to +125 °C							
PHASE COMPARATOR SECTION							
V_{IH}	HIGH-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	3.15	–	–	V
V_{IL}	LOW-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	–	–	1.35	V
V_{OH}	HIGH-level output voltage on pins PCP_OUT and PCn_OUT	$V_I = V_{IH}$ or V_{IL}					
		$I_O = –20$ μA	4.5	4.4	–	–	V
		$I_O = –4.0$ mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage on pins PCP_OUT and PCn_OUT	$V_I = V_{IH}$ or V_{IL}					
		$I_O = –20$ μA	4.5	–	–	0.1	V
		$I_O = –4.0$ mA	4.5	–	–	0.4	V
I_{LI}	input leakage current in pins SIG_IN and COMP_IN	V_{CC} or GND	5.5	–	–	±45	μA
I_{OZ}	3-state OFF-state current in pin PC2_OUT	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	±10.0	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
VCO SECTION							
V_{IH}	HIGH-level input voltage on pin INH	DC coupled	4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage on pin INH	DC coupled	4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage on pin VCO_OUT	$V_I = V_{IH}$ or V_{IL}					
		$I_O = –20$ μA	4.5	4.4	–	–	V
		$I_O = –4.0$ mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage on pin VCO_OUT	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 20$ μA	4.5	–	–	0.1	V
		$I_O = 4.0$ mA	4.5	–	–	0.4	V
V_{OL}	LOW-level output voltage on pins C1A and C1B	$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	4.5	–	–	0.54	V
I_{LI}	input leakage current in pins INH and VCO_IN	V_{CC} or GND	5.5	–	–	±1.0	μA
GENERAL							
I_{CC}	quiescent supply current (disabled)	pin INH at V_{CC}	5.5	–	–	160.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	other inputs at V_{CC} or GND; $V_I = V_{CC} – 2.1$ V; note 1	4.5	–	–	490	μA

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

Table 1 Unit load coefficient table.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

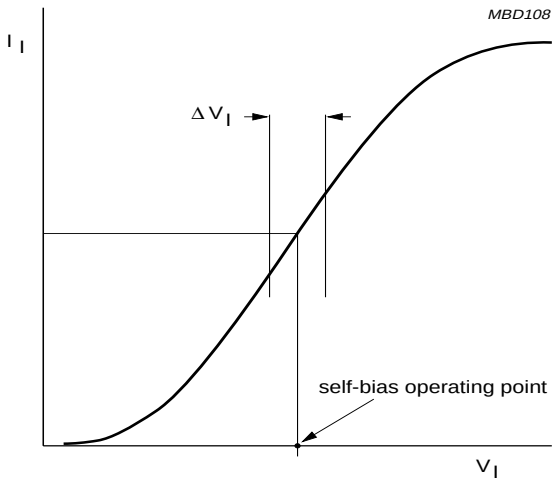


Fig.14 Typical input resistance curve at SIG_IN, COMP_IN.

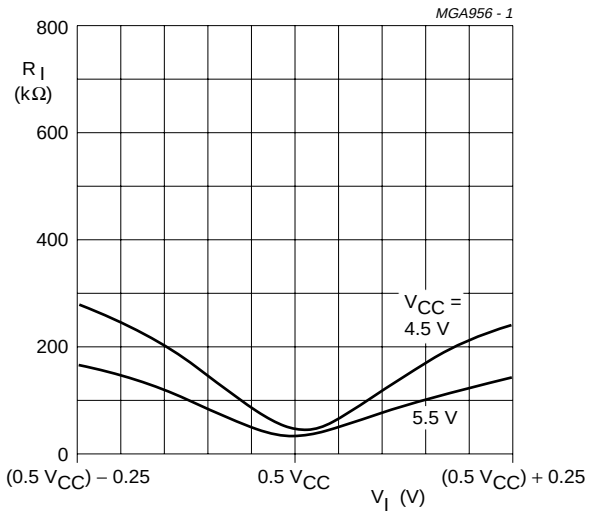


Fig.15 Input resistance at SIG_IN; COMP_IN with ΔV_I = 0.5 V at self-bias point.

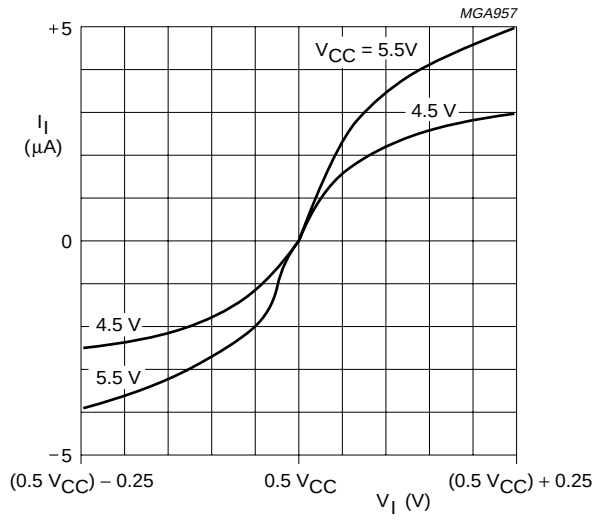
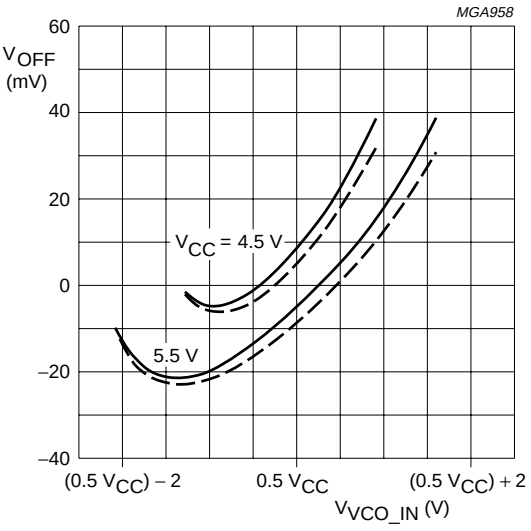


Fig.16 Input current at SIG_IN; COMP_IN with ΔV_I = 0.5 V at self-bias point.



___ R_S = 50 kΩ.
- - - R_S = 300 kΩ.

Fig.17 Offset voltage at demodulator output as a function of VCO_IN and R_S.

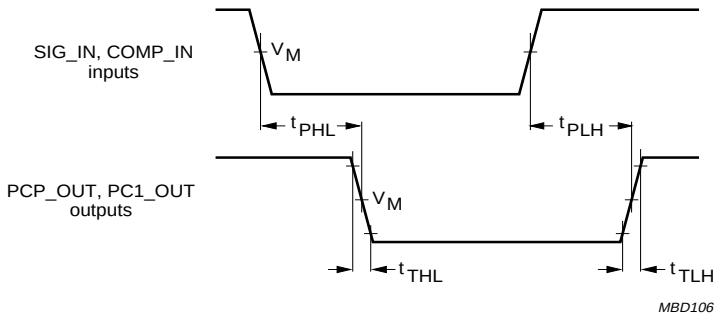
AC CHARACTERISTICS

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
PHASE COMPARATOR SECTION							
t_{PHL}/t_{PLH}	propagation delay SIG_IN, COMP_IN to PC1_OUT	Fig.18	4.5	–	23	40	ns
	propagation delay SIG_IN, COMP_IN to PCP_OUT	Fig.18	4.5	–	35	68	ns
t_{PZH}/t_{PZL}	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	30	56	ns
t_{PHZ}/t_{PLZ}	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	36	65	ns
t_{THL}/t_{TLH}	output transition time	Fig.18	4.5	–	7	15	ns
$V_{i(p-p)}$	input sensitivity at pin SIGN_IN or COMP_IN (peak-to-peak value)	AC coupled; f_i = 1 MHz	4.5	–	15	–	mV
VCO SECTION							
$\Delta f/T$	frequency stability with temperature change	$V_{VCO\_IN} = 0.5V_{CC}$; recommended range: R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF; see Figs 20 to 22	4.5	–	–	–	%/K
Δf_c	centre frequency tolerance	V_{VCO_IN} = 3.9 V; R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF	5.0	–10	–	+10	%
f_c	VCO centre frequency	duty factor = 50%; $V_{VCO\_IN} = 0.5V_{CC}$; R1 = 4.3 kΩ; R2 = ∞; C1 = 40 pF; Figs 23 and 31	4.5	11.0	15.0	–	MHz
Δf_{VCO}	VCO frequency linearity	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; Figs 24 and 25	4.5	–	0.4	–	%
δ_{VCO}	duty factor at VCO_OUT		4.5	–	50	–	%

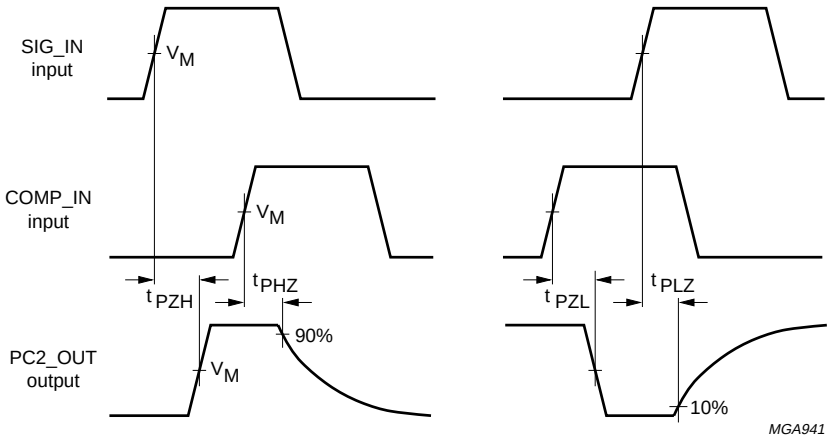
SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
PHASE COMPARATOR SECTION							
t_{PHL}/t_{PLH}	propagation delay SIG_IN, COMP_IN to PC1_OUT	Fig.18	4.5	–	–	50	ns
	propagation delay SIG_IN, COMP_IN to PCP_OUT	Fig.18	4.5	–	–	85	ns
t_{PZH}/t_{PZL}	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	70	ns
t_{PHZ}/t_{PLZ}	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	81	ns
t_{THL}/t_{TLH}	output transition time	Fig.18	4.5	–	–	19	ns
$V_{i(p-p)}$	input sensitivity at pin SIGN_IN or COMP_IN (peak-to-peak value)	AC coupled; f_i = 1 MHz	4.5	–	–	–	mV
VCO SECTION							
$\Delta f/T$	frequency stability with temperature change	V_{VCO_IN} = 0.5V_{CC}; recommended range: R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF; see Figs 20 to 22	4.5	0.06	–	–	%/K
Δf_c	centre frequency tolerance	V_{VCO_IN} = 3.9 V; R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF	5.0	–	–	–	%
f_c	VCO centre frequency	duty factor = 50%; V_{VCO_IN} = 0.5V_{CC}; R1 = 4.3 kΩ; R2 = ∞; C1 = 40 pF; Figs 23 and 31	4.5	–	–	–	MHz
Δf_{VCO}	VCO frequency linearity	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; Figs 24 and 25	4.5	–	–	–	%
δ_{VCO}	duty factor at VCO_OUT		4.5	–	–	–	%

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
PHASE COMPARATOR SECTION							
t_{PHL}/t_{PLH}	propagation delay SIG_IN, COMP_IN to PC1_OUT	Fig.18	4.5	–	–	60	ns
	propagation delay SIG_IN, COMP_IN to PCP_OUT	Fig.18	4.5	–	–	102	ns
t_{PZH}/t_{PZL}	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	84	ns
t_{PHZ}/t_{PLZ}	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	98	ns
t_{THL}/t_{TLH}	output transition time	Fig.18	4.5	–	–	22	ns
$V_{i(p-p)}$	input sensitivity at pin SIGN_IN or COMP_IN (peak-to-peak value)	AC coupled; f_i = 1 MHz	4.5	–	–	–	mV
VCO SECTION							
$\Delta f/T$	frequency stability with temperature change	V_{VCO_IN} = 0.5V_{CC}; recommended range: R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF; see Figs 20 to 22	4.5	–	–	–	%/K
Δf_c	centre frequency tolerance	V_{VCO_IN} = 3.9 V; R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF	5.0	–	–	–	%
f_c	VCO centre frequency	duty factor = 50%; V_{VCO_IN} = 0.5V_{CC}; R1 = 4.3 kΩ; R2 = ∞; C1 = 40 pF; Figs 23 and 31	4.5	–	–	–	MHz
Δf_{VCO}	VCO frequency linearity	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; Figs 24 and 25	4.5	–	–	–	%
δ_{VCO}	duty factor at VCO_OUT		4.5	–	–	–	%



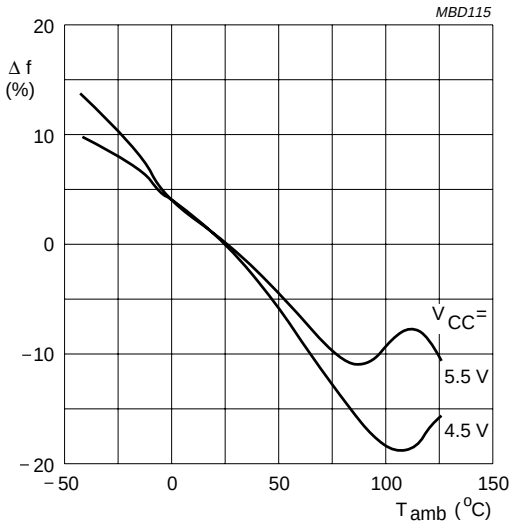
$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

Fig.18 Waveforms showing input (SIG_IN and COMP_IN) to output (PCP_OUT and PC1_OUT) propagation delays and the output transition times.

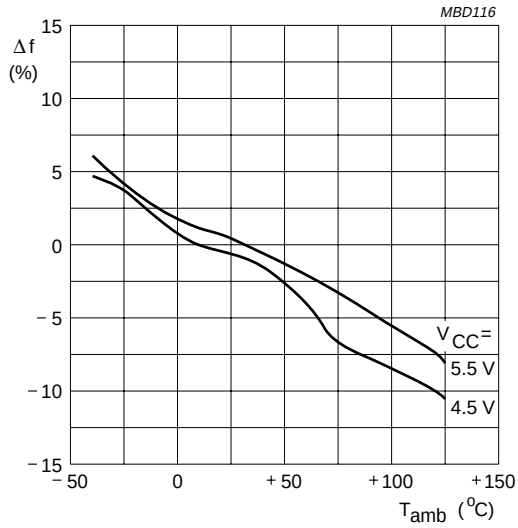


$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

Fig.19 Waveforms showing the 3-state enable and disable times for PC2_OUT.

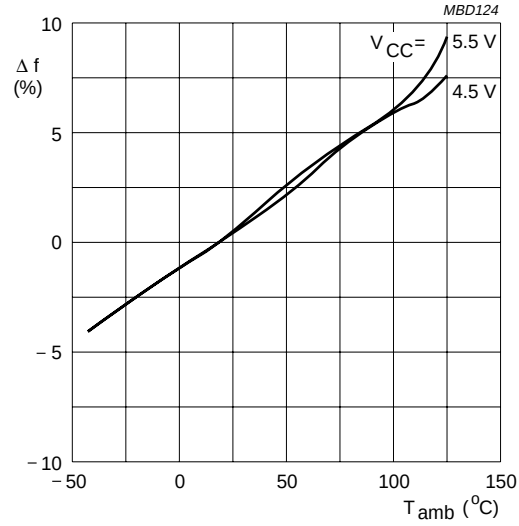


a. R1 = 3 kΩ; R2 = ∞; C1 = 100 pF.

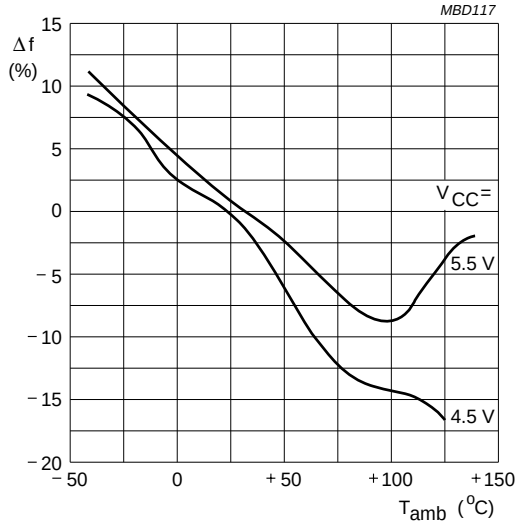


b. R1 = 10 kΩ; R2 = ∞; C1 = 100 pF.

Fig.20 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

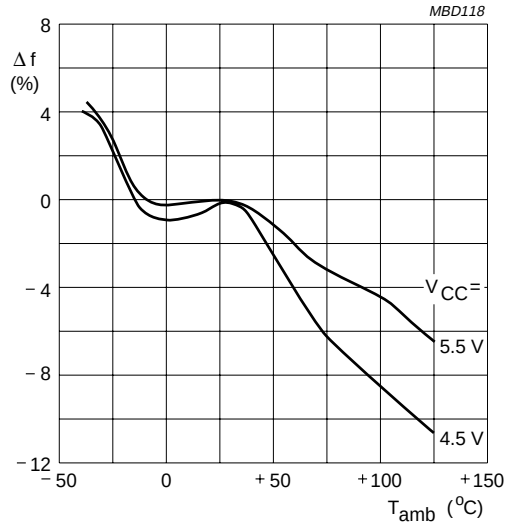


a. R1 = 300 kΩ; R2 = ∞; C1 = 100 pF.

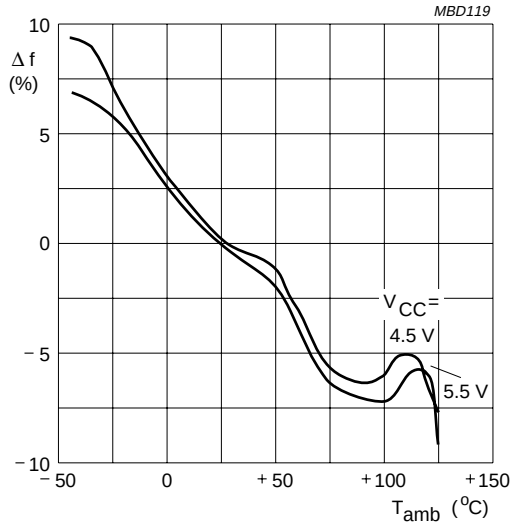


b. R1 = ∞; R2 = 3 kΩ; C1 = 100 pF.

Fig.21 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

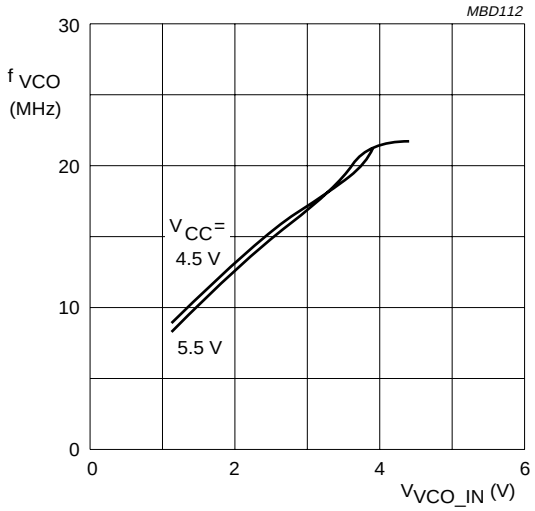


a. R1 = ∞; R2 = 10 kΩ; C1 = 100 pF.

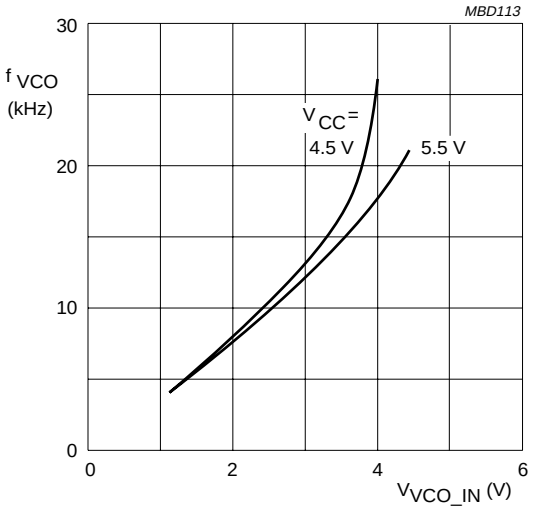


b. R1 = ∞; R2 = 300 kΩ; C1 = 100 pF.

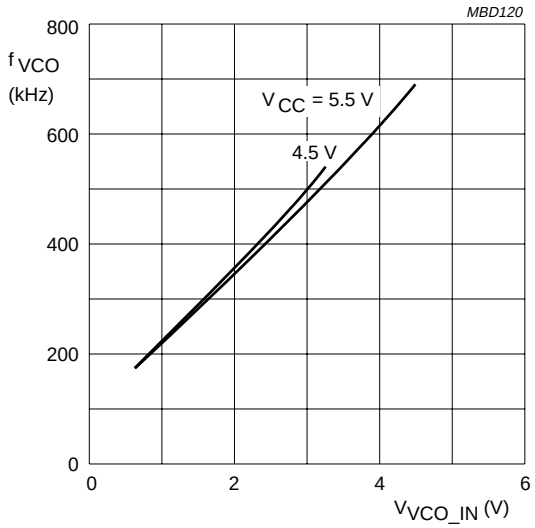
Fig.22 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.



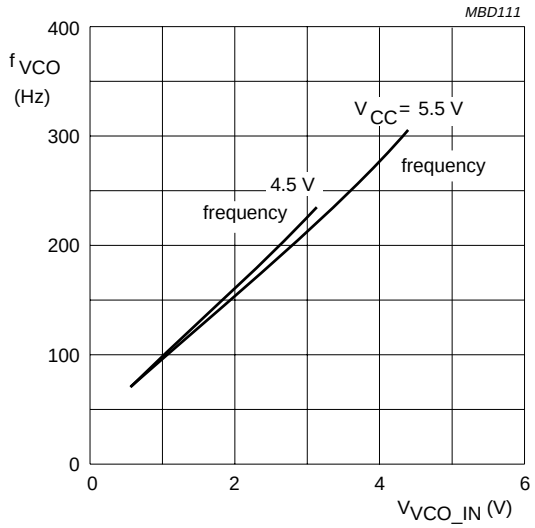
a. R1 = 4.3 kΩ; C1 = 39 pF.



b. R1 = 4.3 kΩ; C1 = 100 nF.

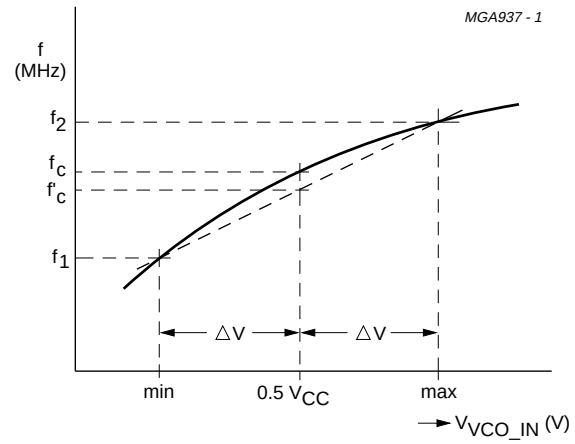


c. R1 = 300 kΩ; C1 = 39 pF.



d. R1 = 300 kΩ; C1 = 100 nF.

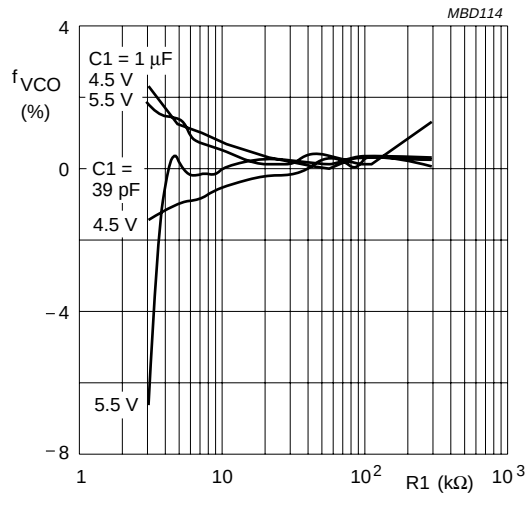
Fig.23 Graphs showing VCO frequency as a function of the VCO input voltage (V_{VCO_IN}).



$$f'_c = \frac{f_1 + f_2}{2}$$

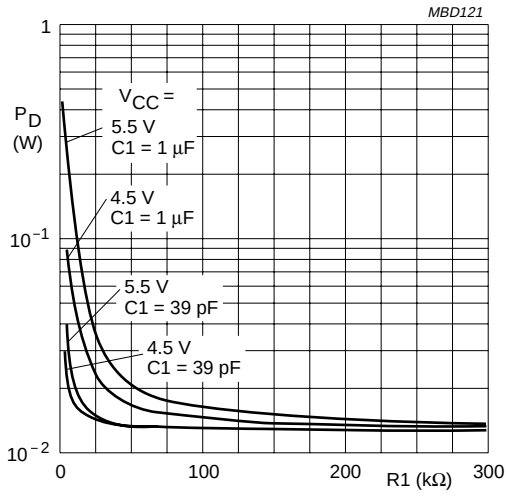
$$\text{linearity} = \frac{f'_c - f_c}{f_c} \times 100\%$$

Fig.24 Definition of VCO frequency linearity: ΔV = 0.5 V over the V_{CC} range.



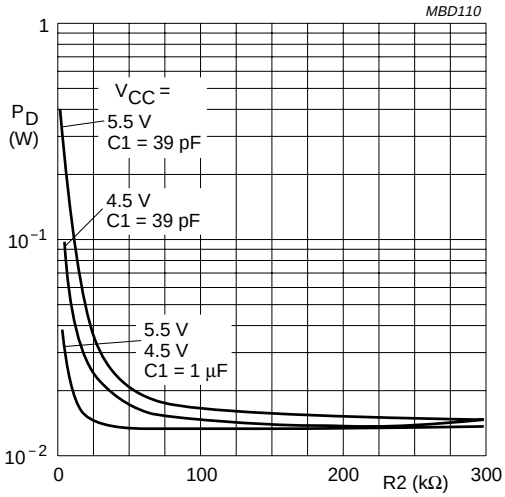
R2 = ∞ and ΔV = 0.5 V.

Fig.25 Frequency linearity as a function of R1, C1 and V_{CC}.



R2 = ∞.

Fig.26 Power dissipation as a function of R1.



R1 = ∞.

Fig.27 Power dissipation as a function of R2.

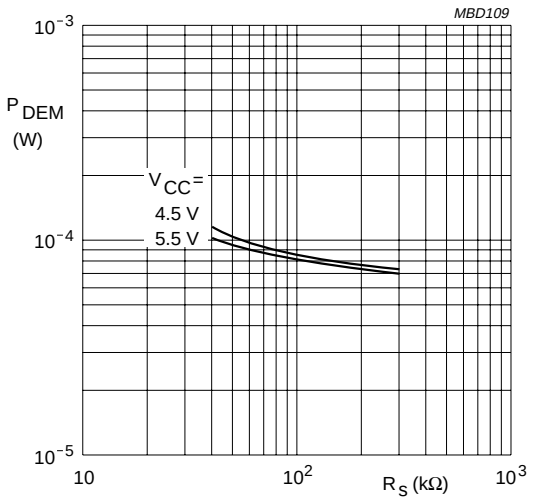


Fig.28 Typical power dissipation as a function of R_S.

APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HCT9046A in a phase-locked-loop system.

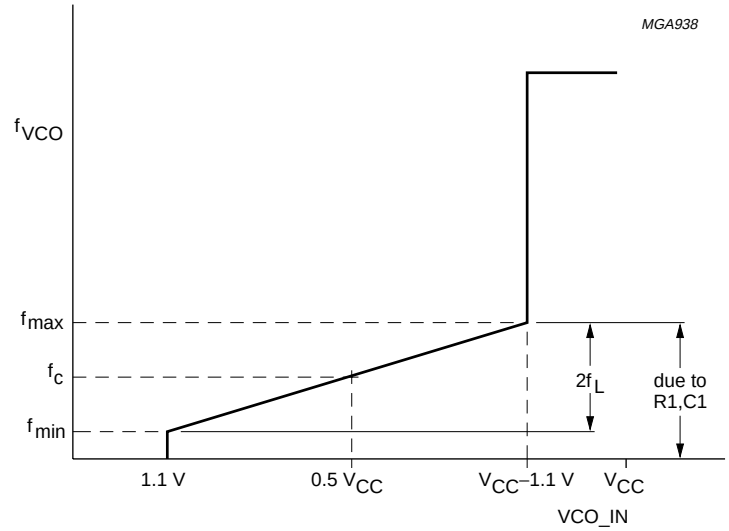
Values of the selected components should be within the ranges shown in Table 2.

Table 2 Survey of components.

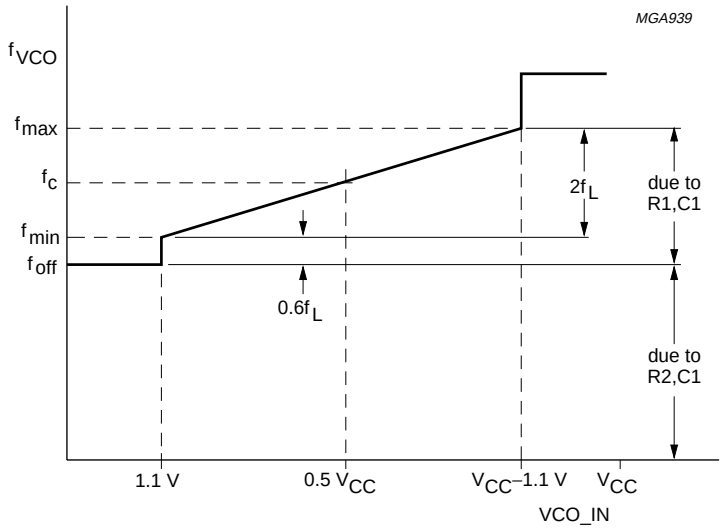
COMPONENT	VALUE
R1	between 3 kΩ and 300 kΩ
R2	between 3 kΩ and 300 kΩ
R1 + R2	parallel value >2.7 kΩ
C1	>40 pF

Table 3 Design considerations for VCO section.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
VCO frequency **without extra offset**	PC1, PC2	VCO frequency characteristic. With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.29a. (Due to R1, C1 time constant a small offset remains when R2 = ∞).
	PC1	Selection of R1 and C1. Given f_c, determine the values of R1 and C1 using Fig.31.
	PC2	Given f_{max} and f_c determine the values of R1 and C1 using Fig.31; use Fig.33 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2	VCO frequency characteristic. With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation is as shown in Fig.29b.
	PC1, PC2	Selection of R1, R2 and C1. Given f_c and f_L determine the value of product R1C1 by using Fig.33. Calculate f_{off} from the equation $f_{off} = f_c - 1.6f_L$. Obtain the values of C1 and R2 by using Fig.32. Calculate the value of R1 from the value of C1 and the product R1C1.
PLL conditions with no signal at pin SIG_IN	PC1	VCO adjusts to f_c with $\Phi_{PC\_IN} = 90°$ and $V_{VCO\_IN} = 0.5V_{CC}$.
	PC2	VCO adjusts to f_{offset} with $\Phi_{PC\_IN} = -360°$ and V_{VCO_IN} = minimum.



a. Operating without offset;
f_c = centre frequency;
$2f_L$ = frequency lock range.



b. Operating with offset;
f_c = centre frequency;
$2f_L$ = frequency lock range.

Fig.29 Frequency characteristic of VCO.

Filter design considerations for PC1 and PC2 of the 74HCT9046A

Figure 30 shows some examples of passive and active filters to be used with the phase comparators of the 74HCT9046A. Transfer functions of phase comparators and filters are given in Table 4.

Table 4 Transfer functions of phase comparators and filters.

PHASE COMPARATOR	EXPLANATION	FIGURE	FILTER TYPE	TRANSFER FUNCTION
PC1	$K_{PC1} = \frac{V_{CC}}{\pi} V/r$	30a.	passive filter without damping	$F_{(j\omega)} = \frac{1}{1 + j\omega\tau_1}$
	$\tau_1 = R3 \times C2$; $\tau_2 = R4 \times C2$; $\tau_3 = R4 \times C3$; $A = 10^5$ = DC gain amplitude	30b.	passive filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$
		30c.	active filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$
PC2	$K_{PC2} = \frac{5}{4\pi} V/r$ $\tau_1 = R3' \times C2$; $\tau_2 = R4 \times C2$; $\tau_3 = R4 \times C3$; $R3' = R_b/17$; R_b = 25 to 250 kΩ	30d.	passive filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ $A = 10^5$ = DC gain amplitude
		30e.	active filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ $A = 10^5$ = DC gain amplitude

General design consideration.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
Noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$; large ripple content at $\Phi_{PC\_IN} = 90°$
	PC2	$f_r = f_i$; small ripple content at $\Phi_{PC\_IN} = 0°$

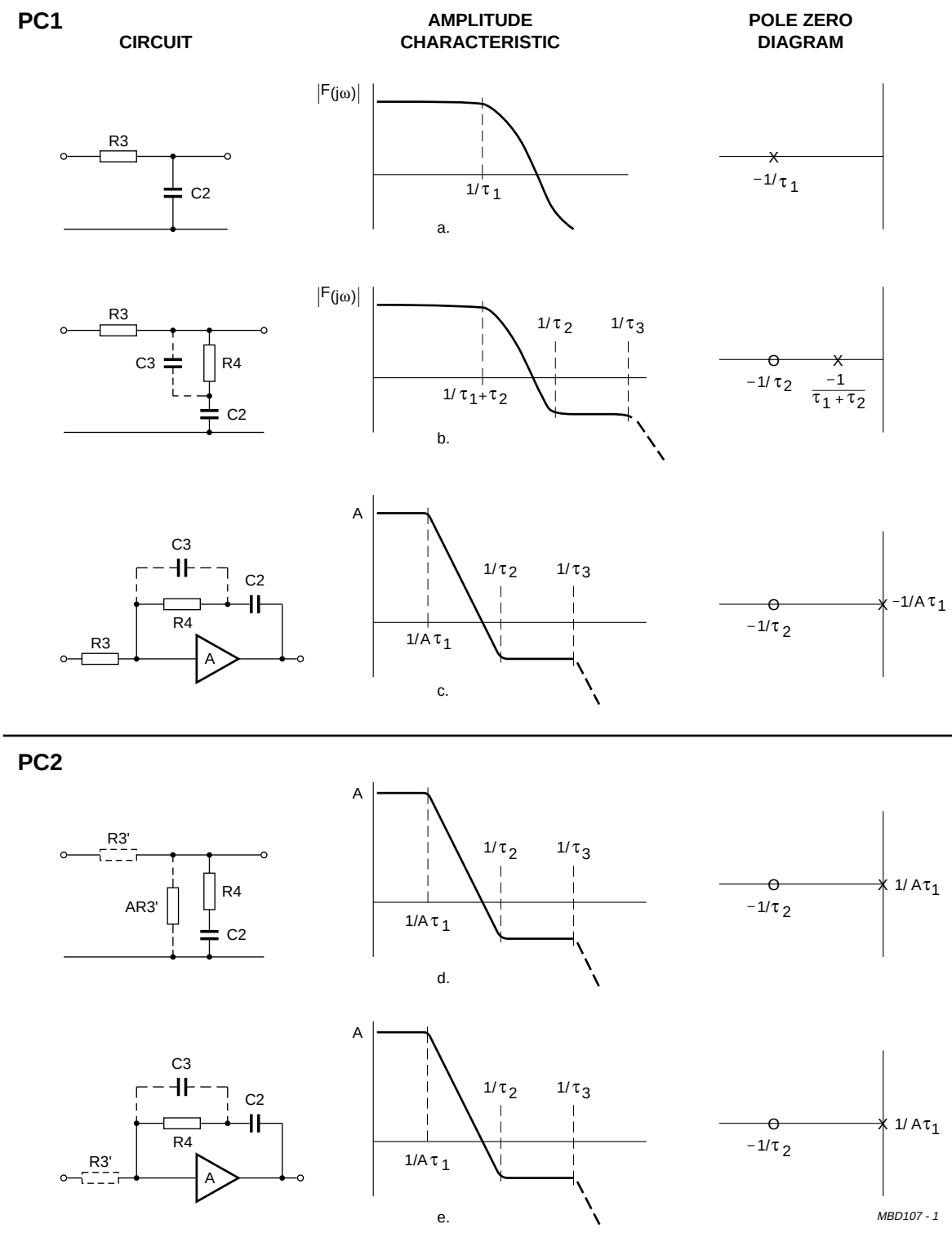
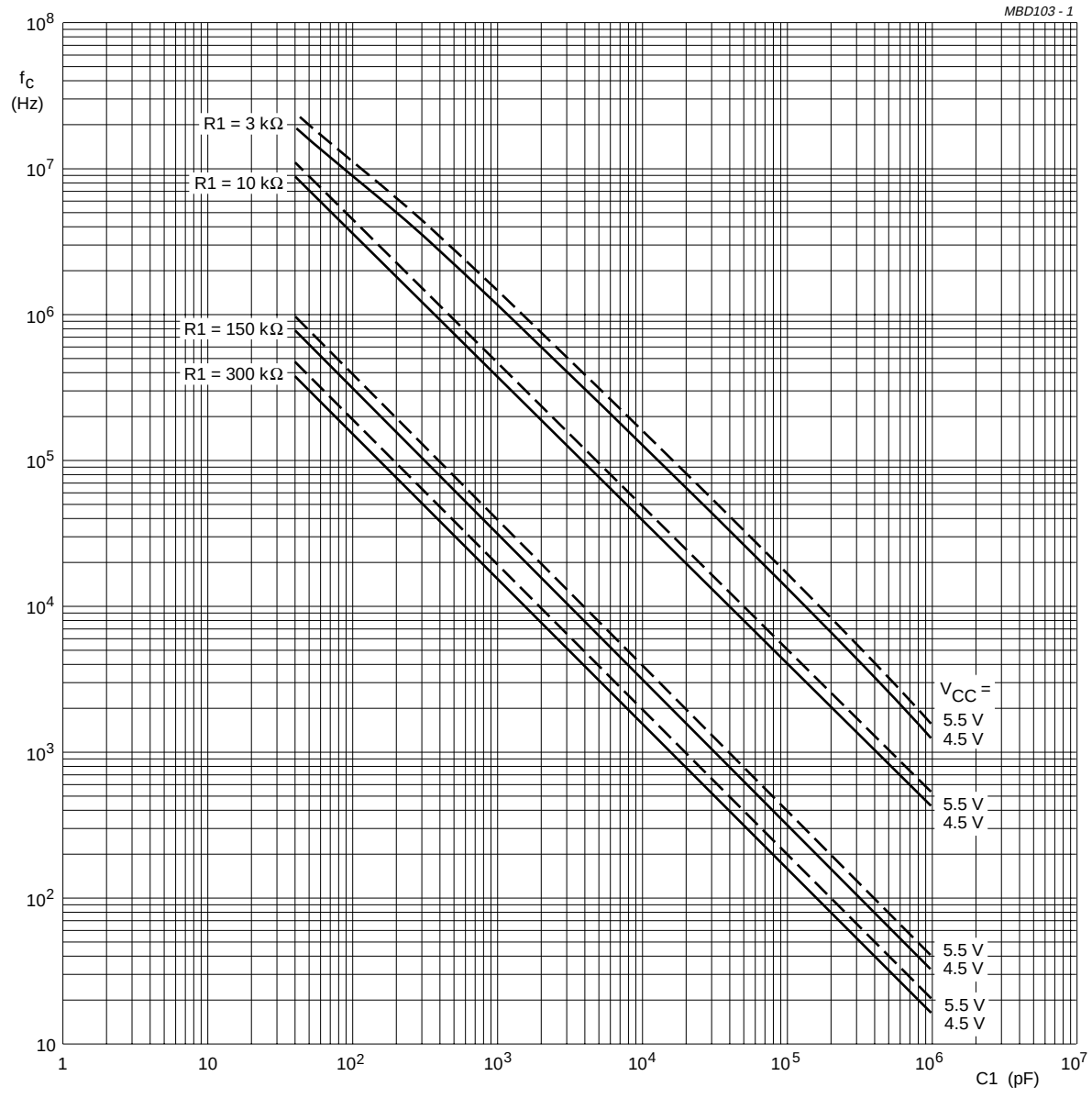
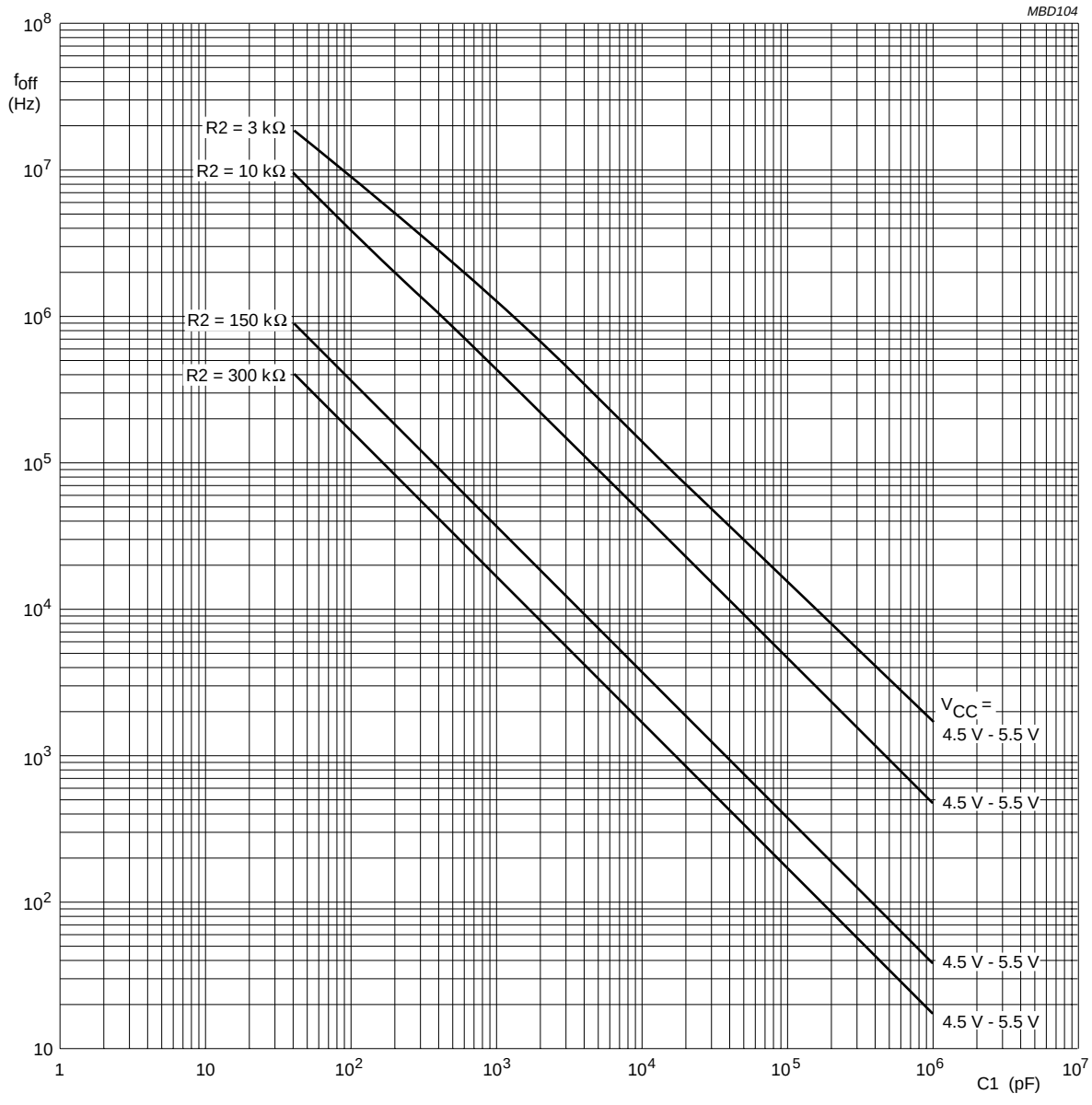


Fig.30 Passive and active filters for 74HCT9046A.



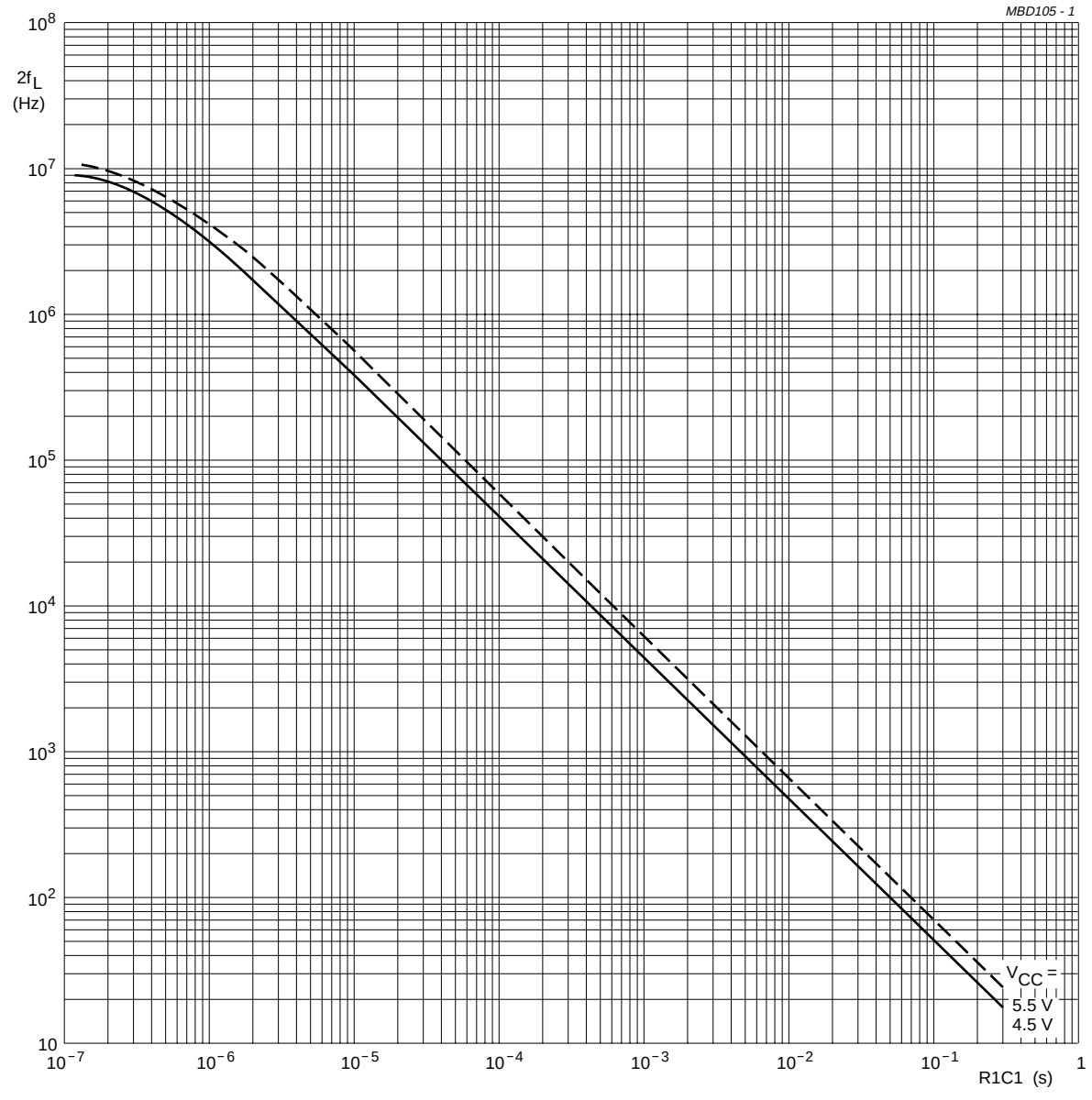
R2 = ∞; V_{VCO_IN} = 0.5V_{CC}; INH = GND; T_{amb} = 25 °C.

Fig.31 Typical value of VCO centre frequency (f_c) as a function of C1.



R1 = ∞; V_{VCO_IN} = 0.5V_{CC}; INH = GND; T_{amb} = 25 °C.

Fig.32 Typical value of frequency offset as a function of C1.



$$K_v = \frac{2f_L}{V_{VCO\_IN}\,range} 2\pi (r/s/V)$$

V_{VCO_IN} = 1.1 to (V_{CC} − 1.1) V.

Fig.33 Typical frequency lock range $2f_L$ as a function of the product R1 and C1.

PLL design example

The frequency synthesizer used in the design example shown in Fig.34 has the following parameters:

Output frequency: 2 MHz to 3 MHz.

Frequency steps: 100 kHz.

Settling time: 1 ms.

Overshoot: <20%.

The open loop gain is:
$H(s) \times G(s) = K_p \times K_f \times K_o \times K_n$

and the closed loop:

$$\frac{\Phi_u}{\Phi_i} = \frac{K_p \times K_f \times K_o \times K_n}{1 + K_p \times K_f \times K_o \times K_n}$$

where:

K_p = phase comparator gain

K_f = low-pass filter transfer gain

$K_o = K_v/s$ VCO gain

$K_n = 1/n$ divider ratio.

The programmable counter ratio K_n can be found as follows:

$$N_{min} = \frac{f_{OUT}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max} = \frac{f_{OUT}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1;
R2 = 10 kΩ (adjustable).

The values can be determined using the information in Table 3.

With f_c = 2.5 MHz and f_L = 500 kHz this gives the following values
(V_{CC} = 5.0 V):

R1 = 30 kΩ.

R2 = 30 kΩ.

C1 = 100 pF.

The VCO gain is:

$$K_v = \frac{2f_L \times 2\pi}{(V_{CC} - 1.1) - 1.1} = \frac{1\ MHz}{2.8} \times 2\pi \approx 2.24 \times 10^6\ r/s/V$$

The gain of the phase comparator PC2 is:

$$K_p = \frac{5}{4 \times \pi} = 0.4\ V/r$$

Using PC2 with the passive filter as shown in Fig.34 results in a high gain loop with the same performance as a loop with an active filter. Hence loop filter equations as for a high gain loop should be used. The current source output of PC2 can be simulated then with a fictive filter resistance:

$$R3' = \frac{R_b}{17}$$

The transfer functions of the filter is given by:

$$K_f = \frac{1 + s\tau_2}{s\tau_2}$$

Where:

$\tau_1 = R3' \times C2$.

$\tau_2 = R4 \times C2$.

The characteristic equation is: $1 + K_p \times K_f \times K_o \times K_n$

This results in:

$$1 + K_p\left(\frac{1 + s\tau_2}{s\tau_1}\right)\frac{K_v}{s}K_n = 0$$

or:

$$s^2 + sK_pK_vK_n\frac{\tau_2}{\tau_1} + K_pK_vK_n/\tau_1 = 0$$

This can be written as:

$$s^2 + 2\zeta\omega_n s + (\omega_n)^2 = 0$$

with the natural frequency ω_n defined as:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{\tau_1}}$$

and the damping value given as: $\zeta = 0.5 \times \tau_2 \times \omega_n$

In Fig.35 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n. From Fig.35 it can be seen that the damping ratio ζ = 0.707 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s\ .$$

Rewriting the equation for natural frequency results in:

$$\tau_1 = \frac{K_p \times K_v \times K_n}{(\omega_n)^2}$$

The maximum overshoot occurs at $N_{max} = 30$; hence $K_n = 1/30$:

$$\tau_1 = \frac{0.4 \times 2.24 \times 10^6}{5000^2 \times 30} = 0.0012$$

When C2 = 470 nF, it follows:

$$R3' = \frac{\tau_1}{C2} = \frac{0.0012}{470 \times 10^{-9}} = 2550\ \Omega$$

Hence the current source bias resistance

$R_b = 17 \times 2550 = 43\ k\Omega$.

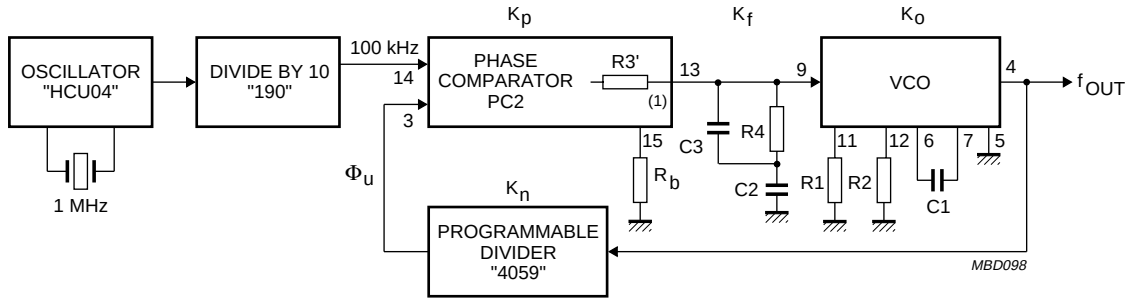
With $\zeta = 0.707$ $(0.5 \times \tau_2 \times \omega_n)$ it follows:

$$\tau_2 = \frac{0.707}{0.5 \times 5000} = 0.00028$$

$$R4 = \frac{\tau_2}{C2} = \frac{0.00028}{470 \times 10^{-9}} = 600\ \Omega$$

For extra ripple suppression a capacitor C3 can be connected in parallel with R4, with an extra $\tau_3 = R4 \times C3$.

For stability reasons τ_3 should be $<0.1\tau_2$, hence $C3 < 0.1C2$ or C3 = 39 nF.



R1 = 30 kΩ.
R2 = 30 kΩ.
R3' = 2550 Ω.
R_b = 43 kΩ.
R4 = 600 Ω.
(1) R3' = fictive resistance

$$R3' = \frac{R_b}{17}$$

C1 = 100 pF.
C2 = 470 nF.
C3 = 39 nF.

Fig.34 Frequency synthesizer.

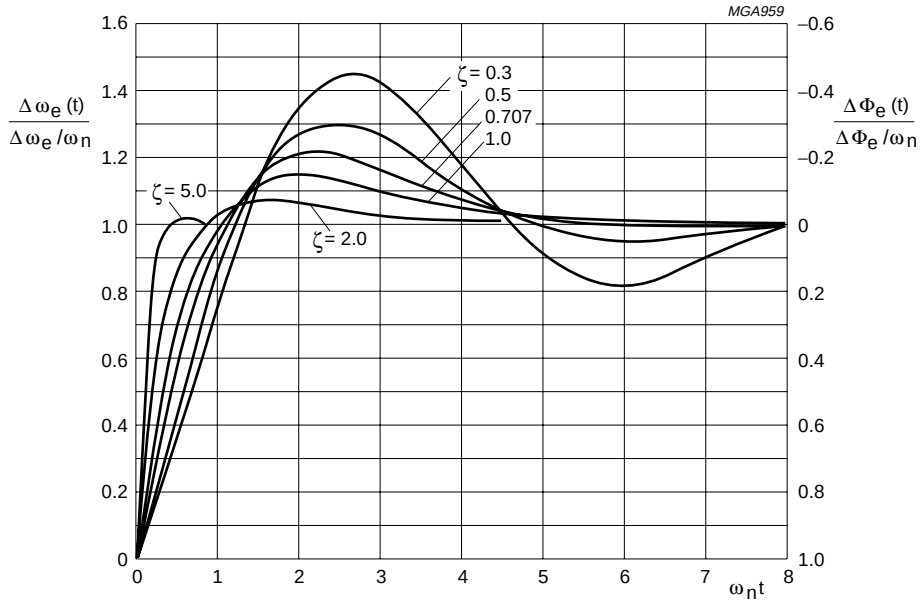


Fig.35 Type 2, second order frequency step response.

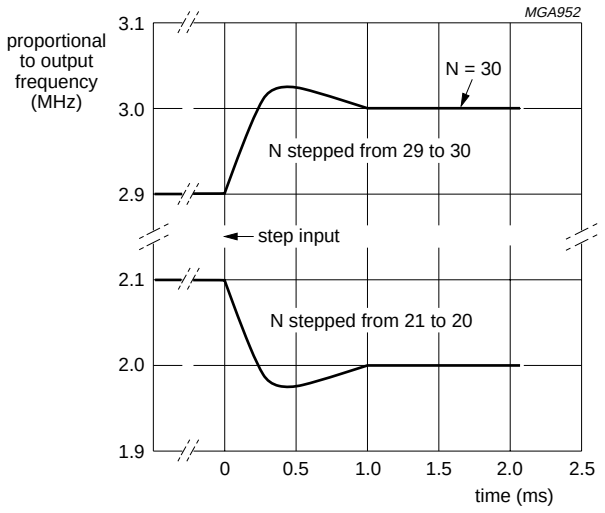


Fig.36 Frequency compared to the time response.

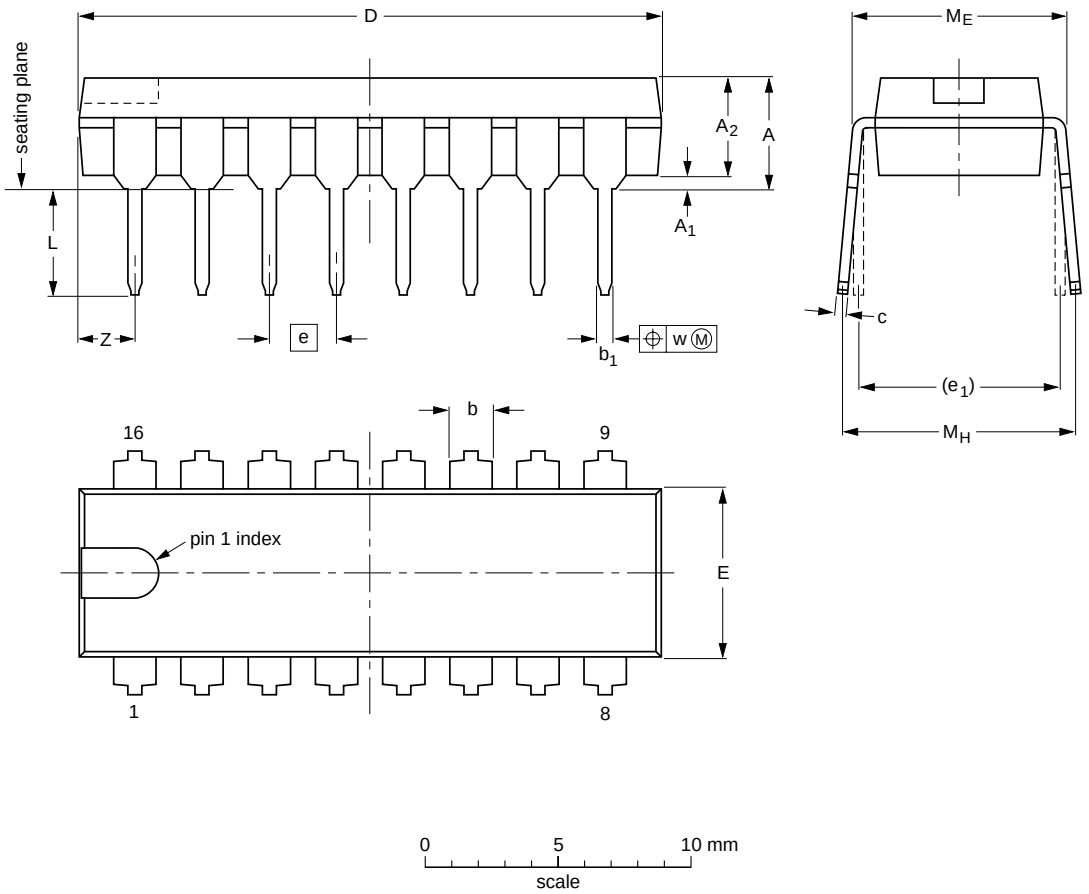
Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin VCO_IN of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin VCO_IN with a simple RC filter, whose time constant is long compared with the phase detector sampling rate but short compared with the PLL response time.

Further information

For an extensive description and application example please refer to *"Application note"* ordering number 9398 649 90011. Also available a *"Computer design program for PLLs"* ordering number 9398 961 10061.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

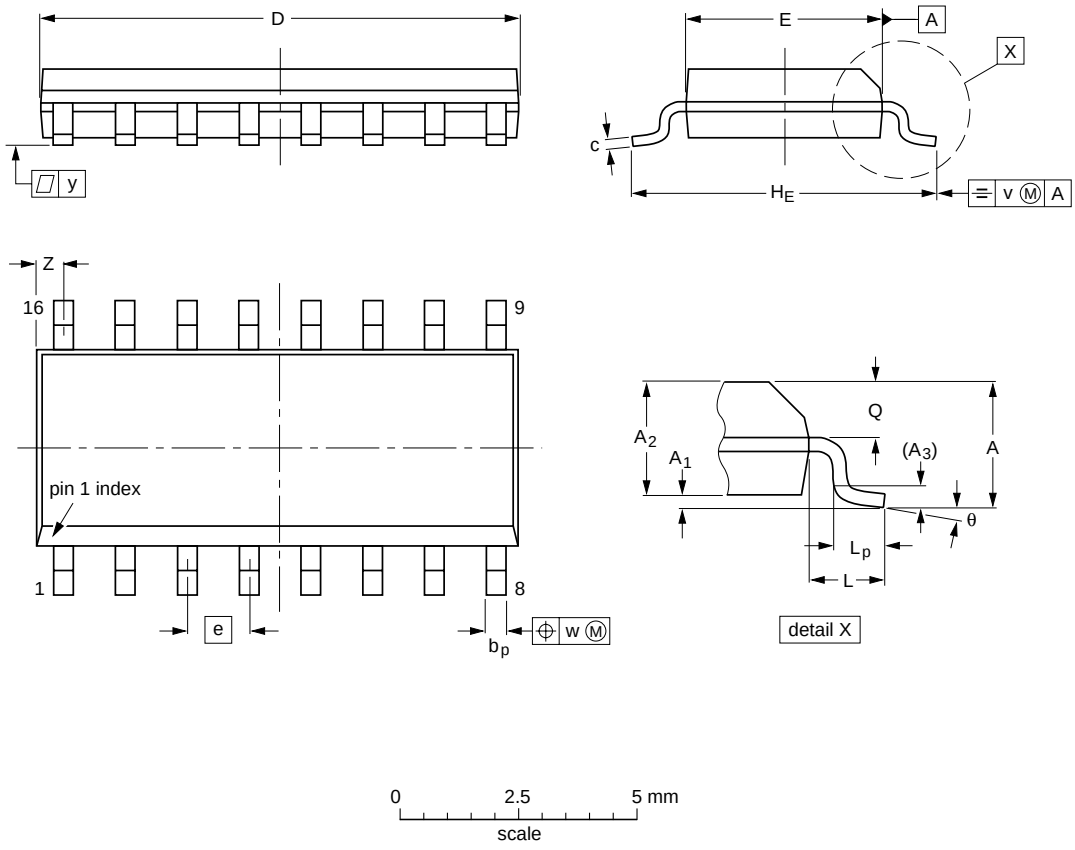
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE[1]	SOLDERING METHOD		
		WAVE	REFLOW[2]	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[3]	–	suitable
Surface mount	BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable	–
	PLCC[5], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[5][6]	suitable	–
	SSOP, TSSOP, VSO	not recommended[7]	suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
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